Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-11: (canceled).

12. (currently amended) A method of fabricating an integrated circuit, comprising the steps of:

forming a dielectric layer over a semiconductor body;

forming a trench in a first part of said dielectric layer;

forming a via in a second part of said dielectric layer;

depositing a liner/barrier layer over said dielectric layer including in said trench and in said via using physical vapor deposition (PVD);

performing a sputter etch of said liner/barrier layer using a low bias after said step of depositing a liner/barrier layer;

depositing a seed layer ~~over~~ on said liner/barrier layer after said step of performing the sputter etch; and

depositing a copper layer over said seed layer.

13. (original) The method of claim 12, wherein said step of depositing a seed layer comprises PVD and occurs prior to said step of performing a sputter etch.

14. (original) The method of claim 12, wherein said steps of forming the liner/barrier layer and forming the seed layer create an overhang portion of liner/barrier and seed material and wherein said sputter etch step reduces thickness of said overhang portion.

15. (original) The method of claim 12, wherein said liner/barrier layer comprises a material selected from the group consisting of Ti, TiN, Ta, TaN, TiNSi, WN, TaNSi, MoN.

16. (original) The method of claim 12, wherein said low bias is in the range of 0 to 300 volts.

17-22 (Cancelled).